AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (ORIGINAL) A method for generating a plurality of timing constraints for a circuit design, comprising the steps of:

(A) identifying a plurality of clock signals by analyzing said circuit design;

(B) determining a plurality of relationships among said clock signals; and

(C) generating said timing constraints for said circuit design in response to said clock signals and said relationships.

2. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein said plurality of clock signals comprise a test clock signal.

3. (PREVIOUSLY PRESENTED) The method according to claim 1, further comprising the step of:

eliminating a respective timing constraint of said timing constraints for each signal connected to an internal pin for said circuit design that defines a non-clock signal.

4. (PREVIOUSLY PRESENTED) The method according to claim 1, further comprising the step of:

eliminating a respective timing constraint of said timing constraints for each signal connected to an external interface for said circuit design that defines a non-clock signal.

5. (ORIGINAL) The method according to claim 1, wherein step (C) is in further response to a plurality of parameters associated with said clock signals.

6. (ORIGINAL) The method according to claim 5, wherein at least one of said parameters relates to a test clock signal of said clock signals.

7. (PREVIOUSLY PRESENTED) The method according to claim 1, further comprising the step of:

eliminating a respective timing constraint of said timing constraints for each signal of said circuit design that defines a static signal.

8. (ORIGINAL) The method according to claim 1, wherein step (B) comprises the sub-step of:

generating an asynchronous relationship of said relationships between at least two of said clock signals operating asynchronously to each other.

9. (ORIGINAL) The method according to claim 1, wherein step (B) comprises the sub-step of:

generating a fastest clock relationship of said relationships between at least two of said clock signals operating at different speeds between two clock boundaries of said circuit design.

10. (ORIGINAL) The method according to claim 1, wherein step (B) comprises the sub-step of:

generating a multiplexed clock relationship of said relationships between at least two of said clock signals routable through a multiplexer in said circuit design.

11. (ORIGINAL) The method according to claim 1, wherein step (B) comprises the sub-step of:

generating a derivative clock relationship of said relationships between a first of said clock signals that is derived from a second of said clock signals.

12. (ORIGINAL) The method according to claim 1, wherein step (B) comprises the sub-step of:

generating a shared structure relationship of said relationships between a test clock signal of said clock signals and a normal clock signal of said clock signals, each driving a particular structure of said circuit design in different modes for said circuit design.

13. (ORIGINAL) The method according to claim 1, further comprising the step of:

writing said timing constraints among a plurality of files.

14. (ORIGINAL) A method for generating a plurality of timing constraints for a circuit design, comprising the steps of:

(A) identifying a plurality of clock signals by analyzing said circuit design;

(B) querying a user for a plurality of parameters for said clock signals; and

(C) generating said timing constraints in response to said clock signals and said parameters.

15. (ORIGINAL) The method according to claim 14, further comprising the step of:

determining a plurality of relationships among said clock signals, wherein said timing constraints are generated in further response to said relationships.

16. (ORIGINAL) The method according to claim 14, wherein step (B) comprises the sub-step of:

querying said user for a frequency parameter of said parameters for each of said clock signals.

17. (ORIGINAL) The method according to claim 14, wherein step (B) comprises the sub-step of:

querying said user for a timing uncertainty parameter of said parameters for each of said clock signals.

18. (ORIGINAL) The method according to claim 14, wherein said circuit design comprises a gate level design.

19. (ORIGINAL) The method according to claim 14, wherein said circuit design comprises a register transfer language design.

20. (PREVIOUSLY PRESENTED) A storage medium comprising a medium and a computer program for use in a computer to generate a plurality of timing constraints for a circuit design, said medium recording said computer program that is readable and executable by the computer, said computer program including the steps of:

(A) identifying a plurality of clock signals by analyzing said circuit design;

(B) determining a plurality of relationships among said clock signals; and

(C) generating said timing constraints for said circuit design in response to said clock signals and said relationships.

21. (PREVIOUSLY PRESENTED) A storage medium comprising a medium and a computer program for use in a computer to generate a plurality of timing constraints for a circuit design, said medium

recording said computer program that is readable and executable by the computer, said computer program including the steps of:

(A) identifying a plurality of clock signals by analyzing said circuit design;

(B) querying a user for a plurality of parameters for said clock signals; and

(C) generating said timing constraints in response to said clock signals and said parameters.